IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1 and amend claims 2, 4, 6-7, as follows:

1. (Cancelled)

2. (Currently Amended) The data storage element ~~according to claim 1, further~~ comprising:

a primary data input;

a primary clock input for selecting storage of a level of the primary data input;

an alternate data input, wherein the alternate data input is received by an inverter-style branch circuit;

an alternate clock input for selecting storage of a level of the alternate data input; and

a first latch element for storing one of the primary data input and the alternate data input, the first latch element comprising:

a totem pole circuit including of at least six transistors, wherein two of the six transistors have a gate signal derived from the primary clock input and two of the six transistors have a gate signal derived from the alternate clock input.

3. (Original) The data storage element according to claim 2, further comprising a second latch element, wherein the second latch element selectively stores an output of the first latch element and the second latch element comprises a second latch data input circuit comprising a transmission gate.

4. (Currently Amended) The data storage element ~~according to claim 1,~~ comprising:

a primary data input;

a primary clock input for selecting storage of a level of the primary data input;

an alternate data input, wherein the alternate data input is received by an inverter-style branch circuit; and

an alternate clock input for selecting storage of a level of the alternate data input,

wherein at least one of the alternate data input and the alternate clock input comprise circuits with lower bandwidths than at least one of the primary data input and the primary clock input.

5. (Original) The data storage element according to claim 4, wherein an input circuit of at least one of the alternate data input and the alternate clock input comprise transistors with higher pass resistance than an input circuit of at least one of the primary data input and the primary clock input.

6. (Currently Amended) An arithmetic unit comprising:

a data storage element, the data storage element comprising:

a primary data input;

a primary clock input for selecting storage of a level of the primary data input;

an alternate data input, wherein the alternate data input is received by an inverter-style branch circuit; and

an alternate clock input for selecting storage of a level of the alternate data input,

wherein at least one of the alternate data input and the alternate clock input comprise circuits with lower bandwidths than at least one of the primary data input and the primary clock input.

7. (Currently Amended) A library of integrated circuit modules, comprising:

a ~~per~~pre-defined data storage element, the pre-defined data storage element comprising:

a primary data input;

a primary clock input for selecting storage of a level of the primary data input;

an alternate data input, wherein the alternate data input is received by an inverter-style branch circuit; and

an alternate clock input for selecting storage of a level of the alternate data input, wherein at least one of the alternate data input and the alternate clock input comprise

circuits with lower bandwidths than at least one of the primary data input and the primary clock input.

8. (Original) A data storage element, comprising:

a first AND gate with a first input and a second input;

a second AND gate with a first input and a second input;

a third AND gate with a first input, a second input and a third input, wherein the first input of the third AND gate receives a signal corresponding to an inverted signal received by the second input of the first AND gate, the second input of the third AND gate receives a signal corresponding to an inverted signal received by the second input of the second AND gate and the third input receives an output of an inverter; and

a NOR gate for receiving the outputs of each of the first AND gate, the second AND gate and a third AND gate and providing an output that is received by an input of the inverter.

9. (Original) The data storage element according to claim 8, wherein at the first input and the second input of the first AND gate receive an alternate data input and an alternate clock input and comprise circuits with lower bandwidths than the first input and the second input of the second AND gate.

10. (Original) The data storage element according to claim 9, wherein the circuits with lower bandwidth comprise transistors with higher pass resistance than circuits of the first input and the second input of the second AND gate.